ANALOG DEVICES

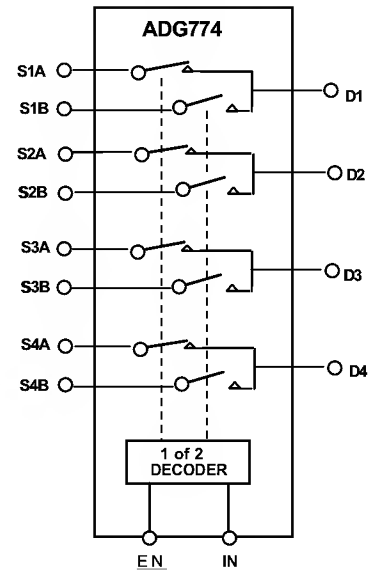
CMOS 3V / 5V, Wide Bandwidth Quad 2:1 Mux

Preliminary Technical Data ADG774

FEATURES
Low insertion loss and On Resistance: 6Ω typical
On Resistance Flatness <2Ω
Single 3.3V/5V supply operation
Rail-to-Rail Operation
Very Low Distortion: 2%
Low Quiescent Supply Current (100nA typical)
Fast Switching Times
t_{ON} 100 ns
t_{OFF} 90 ns
TTL/CMOS Compatible
Pin Compatible with PI5L200

APPLICATIONS
10/100 Base-TX/T4
100VG-AnyLAN
Token Ring 4/16 Mbps
ATM25
NIC Adapter and Hubs
SONET OCI 51.8 Mbps
T1/E1

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG774 is a monolithic CMOS device comprising four independently selectable switches. They are designed on a CMOS process which provides low power dissipation yet gives high switching speed and low on resistance.
The ADG774 is a Rail-to-Rail Quad 2:1 multiplexer/demultiplexer with three-state outputs. With data input of 0V to 5V levels the On-resistance typically varies from 5Ω to 7Ω . This device can be used to replace mechanical relays in low voltage (3.3V/5V systems) LAN applications .

The ADG774 has a wide bandwidth of 135MHz, and so can switch fast ethernet and ATM25 signals. The ADG774 switch distortion is typically less than 2% when switching into 100Ω UTP cables.The ADG774 operates from a single 3.3V/5V supply and is TTL logic compatible.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The control logic for each switch is shown in the Truth Table for the ADG774 on page 4.

These switches conduct equally well in both directions when ON and have an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. The ADG774 switches exhibit break before make switching action . Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Wide bandwidth data rates > 100MHz .
2. Ultralow Power Dissipation
3. Extended Signal Range
   The ADG774 is fabricated on a CMOS process giving an increased signal range which extends fully to the supply rails.
4. Low leakage over temperature.
5. Break Before Make Switching
   This prevents channel shorting when the switches are configured as a multiplexer .
6. Crosstalk
   Crosstalk is typically -70dB @30MHz.

Prelim D 11/97

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Single Supply (V_{DD} = +3.3 V , GND = 0 V, All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B Version +25°C	B Version T_{MIN} to T_{MAX}	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})		15	Ω typ	V_D = 0V to 3V, I_S = –10 mA to -30mA;
		22	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})		1	Ω typ	V_D = 0V to 3 V, I_S = –10 mA;
		3	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)		7	Ω typ	V_D = 0V to V_{DD}, V_{DD}, I_S = –1 mA;
		12	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)		±100	nA max	V_D =3.0 V, V_S = 3.0 V; Test Circuit 2
Drain OFF Leakage I_D (OFF)		±100	nA max	V_D =3.0 V, V_S =3.0 V; Test Circuit 2
Channel ON Leakage I_D, I_S (ON)		±5	nA max	V_D = V_S = 3 V; Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}			µA typ	V_{IN} = V_{INL} or V_{INH}
		±1	µA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}		28	ns typ	R_L = 100 Ω, C_L = 35 pF;
		40	ns max	V_S = +1.5 V; Test Circuit 4
t_{OFF}		4	ns typ	R_L = 100 Ω, C_L = 35 pF;
		20	ns max	V_S = +1.5 V; Test Circuit 4
Break-Before-Make Time Delay, t_D	15		ns typ	R_L = 300 Ω, C_L = 35 pF;
	10	10	ns min	V_{S1} = V_{S2} = +3 V; Test Circuit 5
Off Isolation		-75	dB typ	R_L = 50 Ω, f = 1MHz; Test Circuit?
Channel-to-Channel Crosstalk		-75	dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Bandwidth - 3dB		110	MHz typ	R_L = 50 Ω; Test Circuit ?
Distortion		4	% typ	R_L = 100 Ω
C_S (OFF)		15	pF typ	f = 1 KHz
C_D (OFF)		15	pF typ	f = 1 KHz
C_D, C_S (ON)		TBD	pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +3.6 V Digital Inputs = 0 V or V_{DD}
I_{DD}		1	µA max	
I_{IN}		1	µA max	V_{IN}= +3.0 V
I_O		100	mAmax	V_S/V_D = 0V

NOTES
[1]Temperature ranges are as follows: B Versions: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply (V_{DD} = +5.0 V ± 10%, GND = 0 V, All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B Version +25°C	B Version T_{MIN} to T_{MAX}	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})		6	Ω typ	V_D = 0V to 5V, I_S = –10 mA to -30mA;
		12	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})		0.4	Ω typ	V_D = 0V to 5 V, I_S = –10 mA;
		2	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)		3	Ω typ	V_D = 0V to 5V, V_{DD}, I_S = –1 mA;
		5	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)		±100	nA max	V_D =4.5 V, V_S = 4.5 V; Test Circuit 2
Drain OFF Leakage I_D (OFF)		±100	nA max	V_D =4.5 V, V_S =4.5 V; Test Circuit 2
Channel ON Leakage I_D, I_S (ON)		±5	nA max	V_D = V_S = 4.5 V; Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}			µA typ	V_{IN} = V_{INL} or V_{INH}
		±1	µA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}		10	ns typ	R_L = 100 Ω, C_L = 35 pF;
		20	ns max	V_S = +3.0 V; Test Circuit 4
t_{OFF}		5	ns typ	R_L = 100 Ω, C_L = 35 pF;
		10	ns max	V_S = +3.0 V; Test Circuit 4
Break-Before-Make Time Delay, t_D	15		ns typ	R_L = 300 Ω, C_L = 35 pF;
	10	10	ns min	V_{S1} = V_{S2} = +5V; Test Circuit 5
Off Isolation		-55	dB typ	R_L = 100 Ω, f = 30MHz; Test Circuit?
Channel-to-Channel Crosstalk		-70	dB typ	R_L = 100 Ω, C_L = 5 pF, f = 30 MHz; Test Circuit 8
Bandwidth - 3dB		137	MHz typ	R_L = 100 Ω; Test Circuit ?
Distortion $\Delta R_{ON}/R_L$		2	% typ	R_L = 100 Ω
C_S (OFF)		13	pF typ	f = 1 KHz
C_D (OFF)		13	pF typ	f = 1 KHz
C_D, C_S (ON)		TBD	pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +5.5V Digital Inputs = 0 V or V_{DD}
I_{DD}		1	µA max	
I_{IN}		1	µA max	V_{IN} = +5.0 V
I_O		100	mAmax	V_S/V_D = 0V

NOTES
[1]Temperature ranges are as follows: B Versions: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Truth Table

$\overline{E}$	IN	D1	D2	D3	D4	Function
1	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	DISABLE
0	1	S1A	S2A	S3A	S4A	IN = 0
0	1	S1B	S2B	S3B	S4B	IN = 1

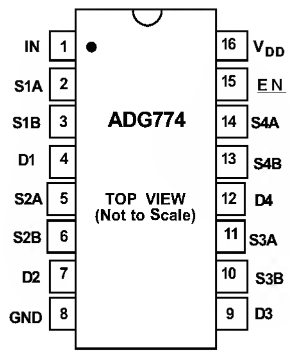
ORDERING GUIDE

Model[1]	Temperature Range	Package Option[1]
ADG774BR	–40°C to +85°C	R-16A
ADG774BRQ	–40°C to +85°C	RQ-16

NOTES

[1] R = 0.15" Small Outline IC (SOIC);RQ= 0.15" Quality Small Outline Package (QSOP)

PIN CONFIGURATION (SOIC/QSOP)



ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . –0.3 V to +7 V
Analog, Digital Inputs[2] . . . . –0.3V to V_{DD} +0.3 V or 30 mA, Whichever Occurs First
Continuous Current, S or D . . . . 100 mA
Peak Current, S or D . . . . 300 mA
(Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range
  Industrial (B Version) . . . . –40°C to +85°C
Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature . . . . +150°C

SOIC Package, Power Dissipation . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . 100°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infrared (15 sec) . . . . +220°C

QSOP Package, Power Dissipation . . . . TBDmW
  θ_{JA} Thermal Impedance . . . . TBD°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infrared (15 sec) . . . . +220°C
ESD 2kV

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG774 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
$\overline{E}$	Logic Control input.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	On resistance match between any two channels i.e. R_{ON}max - R_{ON}min .
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" switch source capacitance.
C_D (OFF)	"OFF" switch drain capacitance.
C_D, C_S (ON)	"ON" switch capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on. See test circuit 4.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_D	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another. See test circuit 5.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Bandwidth	Frequency Response of the awitch in the ON state measured at 3dB down.

Typical Performance Graphs

T.B.D

Figure 1. On Resistance as a Function of V_D (V_S) for various Single Supplies.

T.B.D

Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures with Single Supplies.

T.B.D

Figure 3. Insertion Loss vs. Frequency.

T.B.D

Figure 4. Off Isolation vs. Frequency

T.B.D

Figure 5 . Crosstalk vs. Frequency

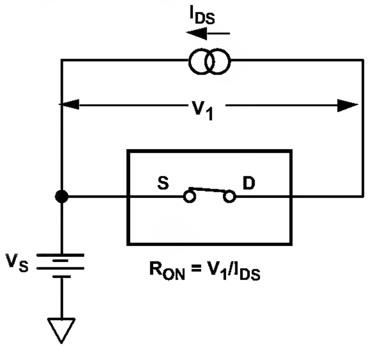
T.B.D

Figure 6 . Total Harmonic Distortion vs. Frequency

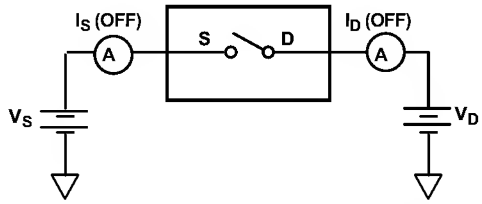
T.B.D

Figure 7. Phase Response with switch on.

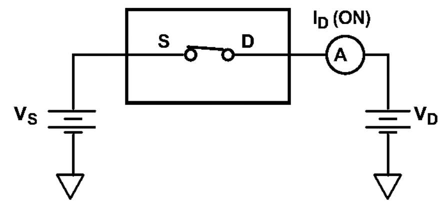
Test Circuits



Test Circuit 1. On Resistance



Test Circuit 2. Off Leakage



Test Circuit 3. On Leakage

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Test Circuit 4. Switching Times

T.B.D

Test Circuit 5. Break-Before-Make Time Delay

T.B.D

Test Circuit 6. Bandwidth

T.B.D

Test Circuit 7. Off Isolation

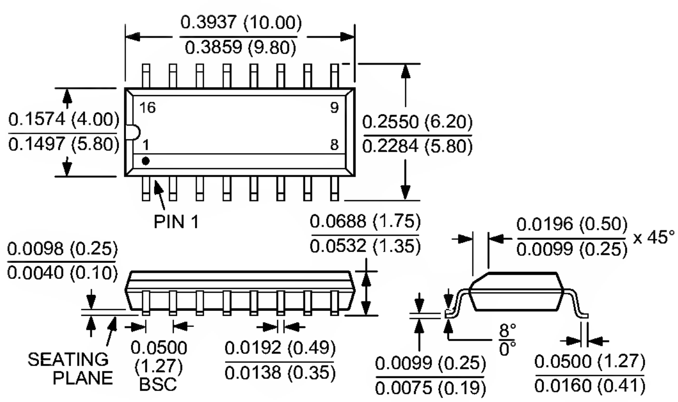
T.B.D

Test Circuit 8. Channel-to-Channel Crosstalk

MECHANICAL INFORMATION

Dimensions are shown in inches and (mm).

16-Pin SOIC (R-16A)



16-Pin QSOP (RQ-16)

T.B.D

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